REMARKS

Claims 1-14 are currently pending in the above-identified application. Claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 are independent.

Interview

The Examiner is thanked for holding an interview on April 23, 2003. Though no agreement was reached, it is believed that the Examiner now has a better understanding of the present invention. As noted in the Examiner's interview summary, the Examiner argued that figure 2 of Brown is packed in a final package form and provides only access to the test pins.

Applicants disagree with the position, as per the arguments presented herein below.

Claim Rejection – 35 U.S.C. 102

Claims 1, 2, 8, and 9 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by Brown et al. (U.S. Patent 5,627,842). Applicants respectfully traverse this rejection.

Brown

Brown is directed to an apparatus and method for centralized boundary-scan fault-testing. Brown's invention is based on the IEEE Std 1149.1 standard. More specifically, Brown is directed to system-wide testing of a multiplicity of integrated circuit modules, e.g., as a plurality of printed circuit boards (column 1, lines 14-19). Brown discloses an example of a prior art test arrangement for a circuit module made up of a number of daisy-chained

interconnected IC chips mounted on a circuit board (shown in Figure 2). In that arrangement, each chip contains a set of pins (Brown, column 3, lines 56-65).

Differences over Brown

The claimed invention, of claims 1, 2, 8, and 9, is directed to a semiconductor device comprising, among other things, a plurality of chips which are "integrally sealed."

The present invention improves over conventional semiconductor devices set up for boundary channel testing by further reducing the total chip area, i.e., providing a smaller package. One feature that enables reduction in the total chip area is a reduction in the total number of pins in the device. Each integrated circuit chip does not have its own set of pins. Thus, the chips are integrally sealed such that the only test pins for the plurality of chips are located at the interface to the integrally sealed semiconductor device.

The Office Action alleges that Figure 2 of Brown teaches a plurality of chips, which are integrally sealed. In particular, the Office Action states that in Brown's Figure 2, "chips are integrally sealed in a circuit board." The Office Action goes on to state that the chips clearly contain IC chips.

> Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. Dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. Denied, 469 U.S. 851 (1984).

At the outset, Brown's Figure 2 is a prior art circuit board arrangement, not even the disclosure of Brown's invention, *per se*. Brown's Figure 2 is briefly described in a paragraph on column 4, as an example IEEE 1149.1 standard-compliant board. In particular, the figure is mentioned in the context of a statement that, "the TCK and TMS leads of the external test bus are connected in parallel to the corresponding TAP pins of all of the individual chips." (column 4, lines 16-19). Applicants submit that there is no mention whatsoever of a final package form of the individual chips. Thus, the allegation that the circuit board of Figure 2 is packed in a final package form with only access to test pins is not inherent within the plain teachings of Brown, and much less taught or suggested by Brown. Therefore, Applicants submit that Brown does not at all disclose a plurality of clips that are integrally sealed. Still further, Brown's Figure 2 explicitly shows a circuit board where each of the individual chips have TAP pins. Thus, Brown's prior art device does not teach a further reduction in size beyond that provided by the standard.

Applicants submit that the Office Action takes a view of the claimed "integrally sealed" that is inaccurate based on the disclosure for the present invention. As can be seen, for example, in Figure 2 of the present invention, chips ic1 and ic2 are integrally sealed air-tight by molded resin (Specification, page 15, lines 7-8). Thus, the meaning of "integrally sealed" as disclosed in the present Specification is that the plurality of chips are sealed air-tight, such as covered by a molded resin, rather than that the chips are bonded to a circuit

board as taught in Brown. Thus, in order to emphasize this distinction, the claims have been amended to include an explicit definition of "integrally sealed" as - integrally sealed air-tight, consistent with the definition provided in the Specification.

Brown's prior art embodiment in figure 2 does not at least disclose this feature, and therefore does not teach each and every claimed element. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. 103

Claims 3-7 and 12-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (U.S. Patent 5,627,842). Applicants respectfully traverse this rejection.

Claim 5 is directed to a similar embodiment as in the above for claim 1. The Office Action admits that Brown does not explicitly teach only one of the chips connected to the test signal input terminal and test signal output terminal whereby the test signal is transferred to the other chips. However, as in the above for claim 1, Applicants submit, however, that Brown does not at least disclose the claimed "semiconductor device in which a plurality of chips are integrally sealed air-tight by molded resin." Brown does not appear to address providing a smaller semiconductor package. Thus, all elements of claim 5 are not taught or suggested by Brown.

Claims 3, 4, and 7 are directed to an embodiment (shown for example in Figure 5) wherein only one of the plurality of chips are connected to the test signal input terminal, the test result output terminal, and control signal input

terminals, and a relay output terminal of the one chip of the first stage is connected to a terminal of a chip of a following stage.

The Office Action directs Applicants attention to statements at column 12, lines 45-65 and column 13, lines 10-20. Those sections disclose the existence of a variety of Boundary-Scan test standards which presumably include the claimed configurations. However, Applicants point out that the present invention is directed at reduction in the size of the total chip area. The present invention accomplishes this by reducing the total number of pins and integrally sealing the plurality of chips. Thus, claim 3 is directed to a configuration in which the plurality of chips is integrally sealed and the terminals/pins consist of a test signal input terminal, test result output terminal, and control signal input terminals connecting to one of the chips. Applicants submit that Brown does not teach such features in reducing the size of the chip. Accordingly, at least for these reasons, Applicants submit that the rejection fails to establish *prima facie* obviousness.

The Office Action admits that Brown does not teach the limitation of a single chip connected to the test signal input terminal, test result output terminal and control signal input terminals, and the one chip successively transferring the test signal and test control signals through other chips. The Office Action instead alleges that Brown's techniques are similar to the applicants' method, such that it would have been obvious to one of ordinary skill in the art to modify Brown's invention to that of the present invention "in order to maximize the system's testing performance." Applicants disagree that

techniques disclosed in Brown are similar to the claimed invention, such that the claimed invention would have been considered an obvious variation.

Brown, as addressed in the above for claim 1, does not teach or suggest a semiconductor device comprising a plurality of chips, which are integrally sealed. Furthermore, Brown does not disclose the claimed arrangement, and much less provide evidence that such an arrangement would maximize testing performance. In particular, Brown does not disclose "only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals." Figure 2 of Brown, for example, shows control signal input terminals TCK and TMS connected to each of the integrated circuits. The arrangement of the present invention of claims 3, 4 and 7 was based on an object to reduce package size. As mentioned above, based on such an arrangement, the TAPC 7 and registers are shared among the chips, enabling chips with fewer numbers of gates, thereby further reducing total chip area as well as package size. Thus, Applicants submit that Brown does not teach or suggest all elements of the claimed invention of claims 3, 4 or 7.

Another feature of the present invention that serves to further reduce the size of the semiconductor device is a fewer total number of pins. In part because the integrated circuit chips are integrally sealed, each integrated circuit chip is interconnected by way of wiring to a pad substrate rather than connecting to a set of pins. In other words, the integrated circuit chips in the semiconductor device do not have a set of pins. On the other hand, in the

device of Brown's figure 2, all of the individual chips have, for example, "TAP pins" (Brown at column 4, lines 16-19). This distinction was emphasized in claims 13 and 14.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-14 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By: Charles Gorenstein

Charles Gorenstein
Reg. No.: 29,271

P.O. Box 747
Falls Church, Virginia 22040-0747
Telephone: (703)205-8000

RWD
CG/RWD/kss

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

The claims have been amended as follows:

1. (Amended) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input terminal for receiving an externally supplied test signal;

a test result output terminal for outputting a test result of said plurality of chips to outside; and

control signal input terminals for receiving externally supplied test control signals,

the test signal inputted from said test signal input terminal being successively transferred through said plurality of chips, and

the test control signals inputted from said control signal input terminals being individually supplied to each of said plurality of chips.

3. (Amended) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input terminal for receiving an externally supplied test signal;

a test result output terminal for outputting a test result of said plurality of chips to outside; and

control signal input terminals for receiving externally supplied test control signals,

only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals,

the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside, and

the test control signals being individually supplied from the one of said plurality of chips to each of the other chips.

5. (Amended) A semiconductor device in which a plurality of chips are integrally sealed <u>air-tight</u>, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output terminals connected to said control circuit, and input terminals of signals to be used in the test, which are all mounted on each chip,

a test commands/data input terminal of a device being connected to the test commands/data input terminal of a chip of a first stage, and the test commands/data output terminal of a chip of a preceding stage being serially connected to the test commands/data input terminal of a chip of a following

stage, and the last commands/data output terminal of a chip of a last stage being connected to a test commands/data output terminal of the device, and input terminals of the device for the signals to be used in the test being connected to the corresponding input terminals of the signals of each chip.

6. (Amended) A semiconductor device in which a plurality of chips are integrally sealed <u>air-tight</u>, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output terminals connected to said control circuit, and input terminals of signals, connected to said control circuit, to be used in the test, which are all mounted on each chip,

a test commands/data input terminal of a device being connected to the test commands/data input terminal of a chip of a first stage, and the test commands/data output terminal of a chip being connected to a corresponding output terminal of the device and serially to the test commands/data input terminal of a chip of a following stage via the output terminal of the device, and input terminals of the device for the signals to be used in the test being connected to the corresponding input terminals of the signals of each chip.

7. (Amended) A semiconductor device in which a plurality of chips are integrally sealed <u>air-tight</u>, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling the test register for testing the chip, test commands/data relay input and output terminals connected to said control circuit, and output terminals of signals to be used in the test outputted from the control circuit, which are all mounted on a chip of a first stage,

test commands/data input and output terminals of a device being respectively connected to the test commands/data input and output terminals of the chip of the first stage, and the relay output terminal of the chip of the first stage being connected to a test commands/data input terminal of a chip of a following stage, and a test commands/data output terminal and a test commands/data input terminal being serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output terminal of a chip of a last stage being connected to the relay input terminal of the chip of the first stage so as to form a loop, and the output terminals of the chip of the first stage for the signals to be used in the test being connected to input terminals of the signals of the other chips.

8. (Amended) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed <u>air-tight</u>;

a test signal input pin for receiving an externally supplied test signal;

a test result output pin for outputting a test result of said plurality of chips to outside; and

control signal input pins for receiving externally supplied test control signals,

the test signal inputted from said test signal input pin being successively transferred through said plurality of chips connected with each other by wires sealed with said plurality of chips, and

the test control signals inputted from said control signal input pins being individually supplied to each of said plurality of chips via wires sealed with the plurality of chips.

10. (Amended) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input pin for receiving an externally supplied test signal;

a test output pin for outputting a test result of said plurality of chips to outside; and

control signal input pins for receiving externally supplied test control signals,

only one of said plurality of chips being connected to said test signal input pin, to said test result output pin, and to said control signal input pins,

the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips so connected to each other by wires sealed with the plurality of chips, and after being inputted again into the one of said plurality of chips, outputted as the test result to outside, and

the test control signals being individually supplied from the one of said plurality of chips to each of the other chips via wires sealed with the plurality of chips.

12. (Amended) A semiconductor device in which a plurality of chips are integrally sealed air-tight, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output pads connected to said control circuit, and input pads of signals to be used in the test, which are all mounted on each chip, wherein

a test commands/data input pin of a device is connected to the test commands/data input pad of a chip of a first stage, and the test commands/data output pad of a chip of a preceding stage is serially connected to the test commands/data input pad of a chip of a following stage, and the test commands/data output pad of a chip of a last stage is connected to a test commands/data output pin of the device, and input pins of the device for the signals to be used in the test is connected to the corresponding input pads of the signals of each chip, connection being performed via wires sealed with the plurality of chips.

13. (Amended) A semiconductor device in which a plurality of chips are integrally sealed air-tight, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output pads connected to said control circuit, and input pads of signals, connected to said control circuit, to be used in the test, which are all mounted on each chip, wherein

a test commands/data input pin of a device is connected to the test commands/data input pad of a chip of a first stage, and the test commands/data output pad of each chip is connected to a corresponding output pins of the device and serially to the test commands/data input terminal of a chip of a following stage via the output pin of the device, and input pins of the device for the signals to be used in the test is connected to the corresponding input pins of the signals of each chip, connection being performed via wires sealed with the plurality of chips.

14. (Amended) A semiconductor device in which a plurality of chips are integrally sealed <u>air-tight</u>, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling the test register for testing the chip, test commands/data relay input and output pads connected to said control circuit, and output pads of signals to be used in the test outputted from the control circuit, which are all mounted on a chip of a first stage, wherein

test commands/data input and output pins of a device is respectively connected to the test commands/data input and output pads of the chip of the first stage, and the relay output pad of the chip of the first stage is connected to a test commands/data input pad of a chip of a following stage, and a test commands/data output pad and a test commands/data input pad is serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output pad of a chip of a last stage is connected to the relay input pad of the chip of the first stage so as to form a loop, and the output pads of the chip of the first stage for the signals to be used in the test is connected to input pads of the signals of the other chips, connection being performed via wires sealed with the plurality of chips.